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The attached report describes development of wideband delta sigma ADCs using high speed Indium Phosphide bipolar transistors.

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# High Resolution Transferred Substrate HBT Microwave/RF ADCs

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## Introduction

In the proposed program, very high clock frequency $\Delta - \Sigma$ ADCs were proposed as a method of obtaining high effective resolutions over large signal bandwidths. In $\Delta - \Sigma$ ADCs, high resolutions are obtained through a combination of oversampling and noise shaping with frequency-selective feedback; with a typical 2nd-order loop design, each 2:1 increase in the sampling rate relative to the Nyquist frequency increases the effective resolution by 2.5 bits. Target resolution of ADCs in Naval radar systems is in the range of 8-12 bits, with the highest feasible signal bandwidth. Bandwidths as much as 1 GHz might be demanded in a system with high bandwidth.

At the time of program initiation, transferred-substrate HBTs in development at UCSB had a significant bandwidth advantage over competing devices for high speed mixed signal ICs. A program effort was therefore undertaken to realize $\Delta - \Sigma$ ADCs with very high clock frequencies in this technology. The original objective was to obtain sampling rates in the 20-40 GHz range. Together with complex multi-bit internal quantizers, a theoretical resolution of 16 bits at 160 MHz signal bandwidth might be feasible.

Realizable system performance falls far below these goals. First, the limits on fabrication yield in a university process force the circuit complexity to be kept below several hundred transistors, at high level only a single-bit internal quantizer is feasible. Secondly, although the transferred-substrate technology proved to be capable of digital circuit operation at clock frequencies as high as 75 GHz, accurate operation of a latched comparator requires that its clock frequency be well below that the maximum digital clock rate feasible. Consequently, the maximum useful clock frequency obtainable is 10-20 GHz with the current status of high speed InP HBT technology. At this level of performance, 8.3 effective bits resolution is feasible for a 125 MHz bandwidth. While this is a very high resolution for a wideband $\Delta - \Sigma$ ADC, alternative approaches (pipelined Nyquist converters) offer somewhat superior performance.

**Technical Background: theory of delta sigma ADCs**

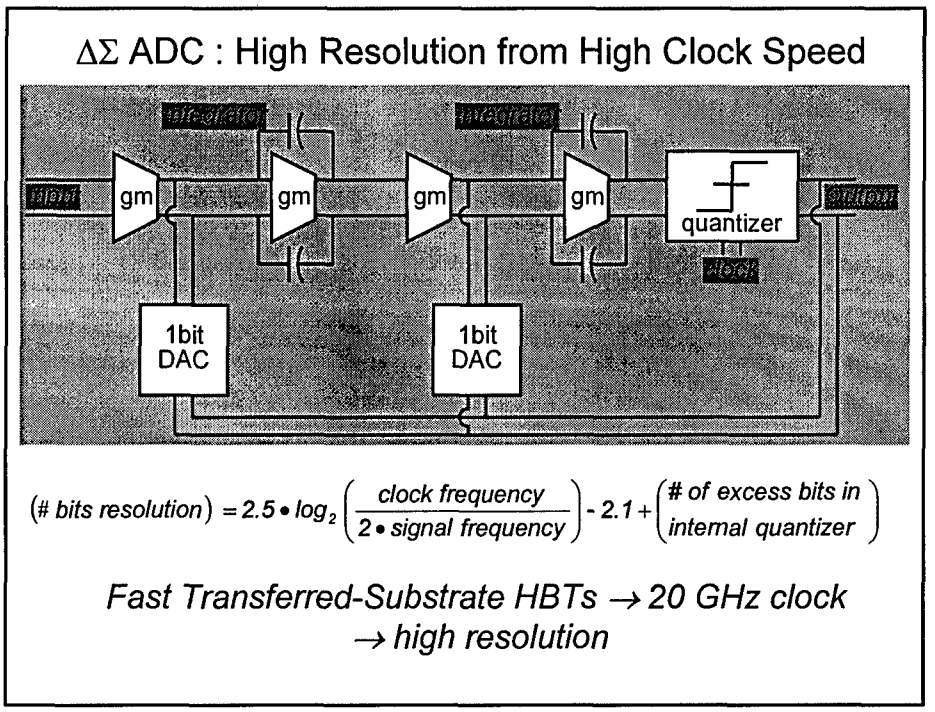



Figure 1: Block Diagram of a $\Delta - \Sigma$ ADC

$\Delta - \Sigma$ ADCs obtain high resolution by placing *negative feedback* around (typically) a one-bit ADC. The output is a rapidly-fluctuating one-bit word whose time-average value accurately represents the input voltage. The frequency response of the 2-integrator feedback loop results in very high feedback loop gain at low frequencies, suppressing quantization noise at any signal frequency in proportion to the loop gain at that frequency. The loop forces the signal power associated with the quantization noise power to be driven to high frequencies, and (mostly) out of the bandwidth of interest. Given a one-bit ADC, quantizers in the ADC must set only a single threshold at zero volts, hence component precision of no relevance. Against this advantage, the $\Delta - \Sigma$ ADC requires very high feedback factors at the signal frequencies of interest, which implies a very high oversampling ratio.

Mathematical theory of the $\Delta - \Sigma$ ADC will not be derived here. The effective number of bits resolution for an ideal $2^{nd}$-order $\Delta - \Sigma$ ADC is given by :

$$\#\text{ bits resolution} = 2.5 \bullet \log_2\left[\frac{clock\_frequency}{2 \times signal\_frequency}\right] - 2.1 + \#\text{ bits in the internal quantizer}$$

The resolution increases at a rate 2.5 times the log of the oversampling ratio as a consequence of (1) the uniform frequency distribution of the quantization noise of the internal quantizer and (2) the gain of the 2-integrator loop varying as $(f_{clock}/f)^2$. If the clock frequency is doubled relative to the signal frequency, the quantization noise power is spread over a 2:1 larger bandwidth, increasing resolution by 1/2 bit, and the loop gain at a given signal frequency is increased 4-fold, increasing the resolution by 2 bit. Thus each 2:1 increase in the clock frequency relative to the signal frequency increases resolution by 2.5 bits.

High resolutions with lower clock frequencies can be obtained if the $\Delta - \Sigma$ modulator contains more than 2 integrators within the feedback loop. ADCs of higher than second order (2 integrators) are extremely prone to limit-cycle oscillations, particularly if only a single-bit internal quantizer is employed. In this manner, bandwidth requirements on the ADC are eased, albeit at the expense of substantially increased circuit design difficulty. In particular, prevention of signal-dependent limit-cycle oscillations generally demands use of limiters within the $\Delta - \Sigma$ feedback loop, which in turn impairs resolution. For demonstrated ADCs, the improvement of resolution with integration orders higher than 2 is not large.

Further improvements in resolution can be obtained using multi-bit quantization with associated error randomization, as is also illustrated in figure 1. With a multi-bit feedback DAC, mismatch errors in the DAC are in the feedback path, and are therefore not suppressed by the loop gain. Errors must therefore instead be suppressed by error randomization techniques. Such circuits, while common in CMOS, have very high transistor counts.

Instead, in this program, higher resolutions were sought through the highest possible clock frequencies. Transferred-substrate HBTs provided at the time record transistor bandwidth and hence offer the potential for the highest $\Delta - \Sigma$ clock frequencies.

**ICs designed**

In this program, two generations of $\Delta - \Sigma$ ADC were ultimately designed, fabricated, and tested. The first was in transferred-substrate technology, and had a 20 GHz clock rate. For this design, resolution fell far below theoretical levels, in part due to dynamic errors arising from metastability effects in the latched comparator. Because it was found that yielding large ICs in the transferred-substrate technology was difficult, the second-generation design was implemented in a more standard and Manufacturable mesa HBT technology. So as to properly interface with available digital instruments, this IC was

also operated at a reduced 8 GHz clock frequency, and showed resolution closer to -but still somewhat below - theoretical predictions.

**First-Generation Delta-Sigma ADC**

The first-generation design was implemented in transferred-substrate HBT technology.

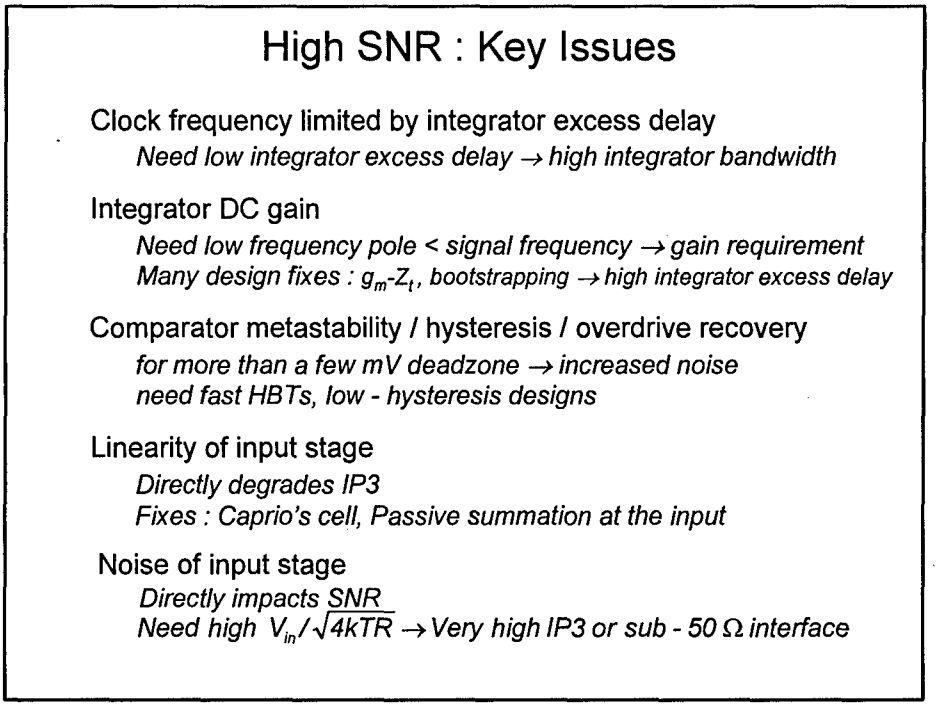



Figure 2: Key issues determining $\Delta - \Sigma$ ADC SNR hence resolution.

Figure 2 highlights the key issues regarding the design of high resolution $\Delta - \Sigma$ ADCs. While high clock rates are potentially feasible up to the maximum frequency at which a latched comparator can be toggled, the highest clock rate at reasonable performance is also limited the excess phase delay in the loop, and by dynamic imperfections in the comparator. These imperfections, which include dynamic hysteresis, metastability, and overdrive recovery time, become progressively more severe as the comparator toggle rate is increased. For this reason, although the transferred-substrate technology at the time could support a ~70 GHz toggle rate, target $\Delta - \Sigma$ clock rates were instead lower at ~20 GHz.

Additional constrains on the performance of the $\Delta - \Sigma$ ADC include the gains of the integrators, and the linearity and noise of the input stage. Ideally, the integrator gain

varies at $f_o / jf$, but the finite input and load resistances of the transistor stages cause the gain to instead be finite at low frequencies. This finite gain limits the degree of in-band noise suppression.

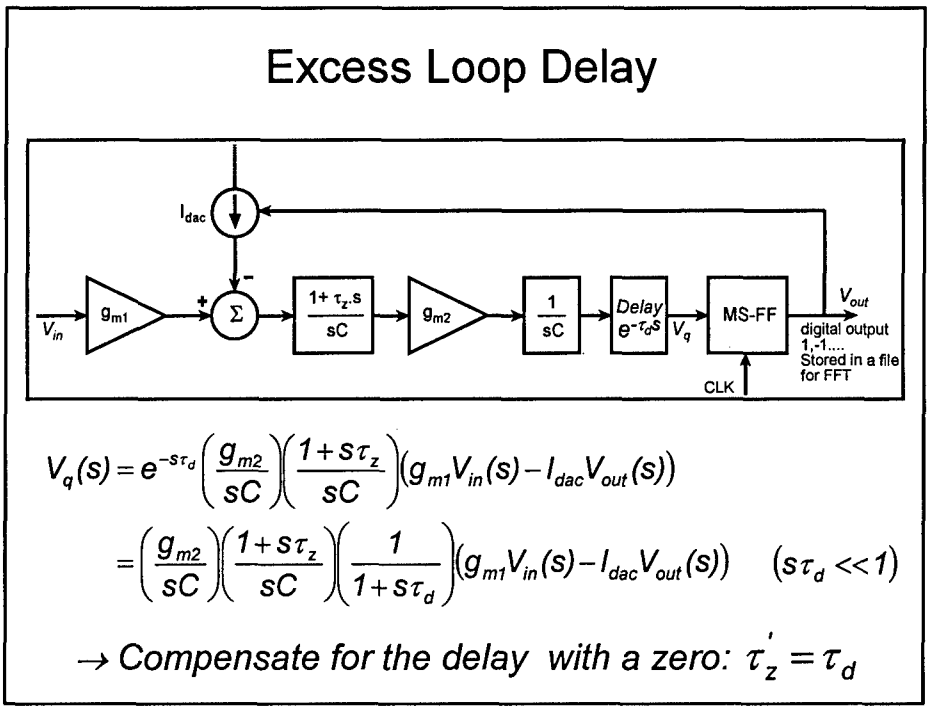



Figure 3: Excess loop delay and the impact on SNR

Excess delay in the forward path (Figure 3) arises from transistor parasitics in the 2 integrators, from delay in the latch, and (if present) from additional delay associated with a 2-stage (MSS) latch. While these effects are predicted by an approximate linearized analysis to have no impact upon the loop noise suppression, exact analysis by MATLAB (fig. 4) shows substantial degradation when the excess delay is of order 10% of the clock period. Introduction of a zero (fig. 3, fig. 4) is an effective method of avoiding this degradation, and is effective for delays as large as 50% of the clock period

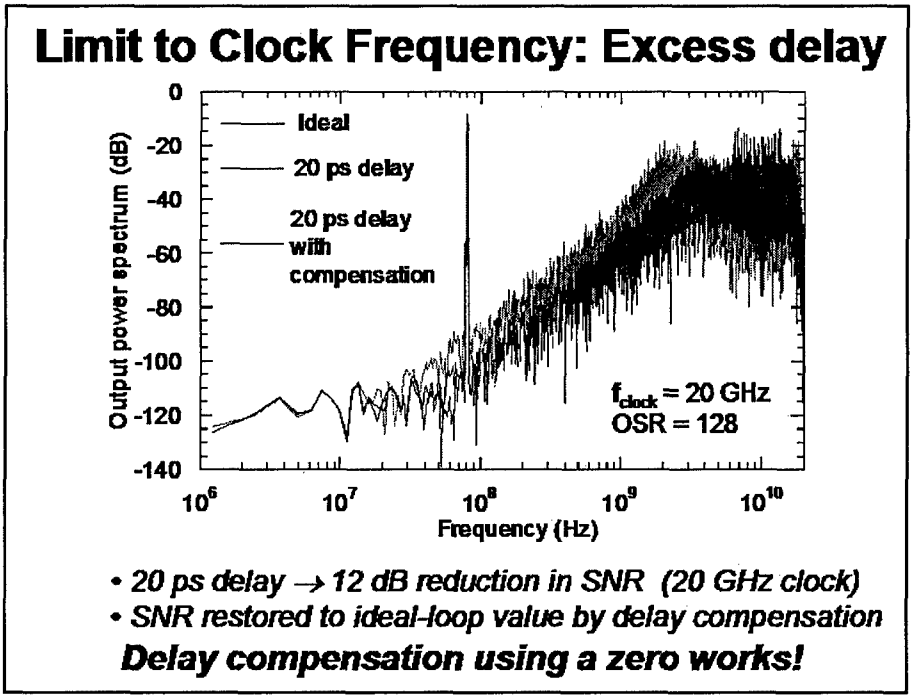



Figure 4: Effect of excess loop delay on SNR

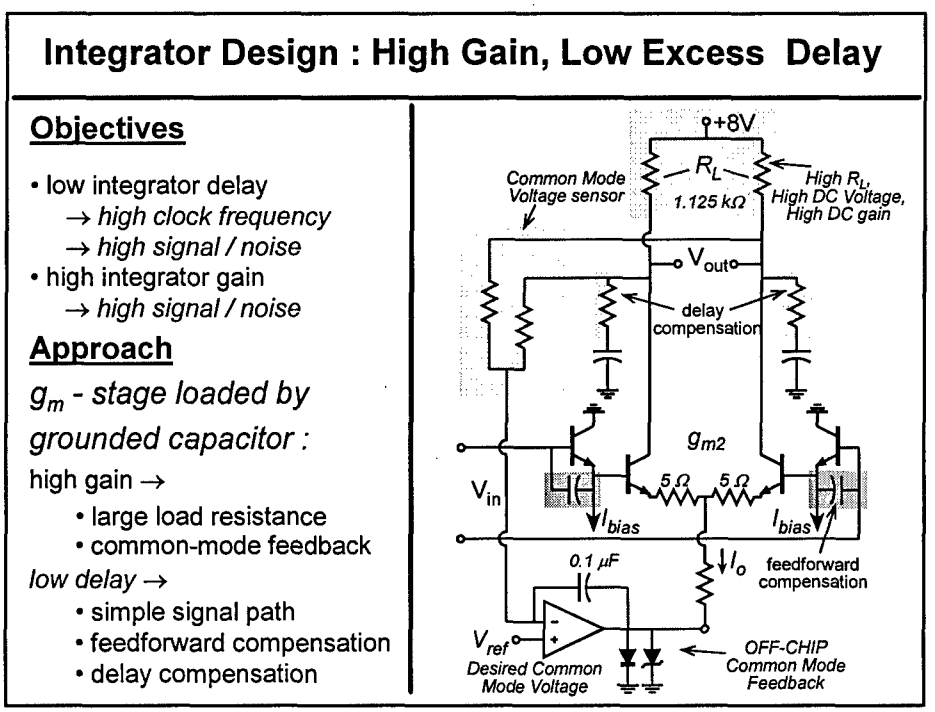



Figure 5: Integrator Design

The integrators within the loop must have high gain at the frequencies at which significant noise suppression is desired; the noise suppression being proportional to the product of the 2 integrators gain at those same frequencies. While HBT processes excel at producing wideband circuits, circuits with high gain at lower frequencies are more challenging due to both the finite DC current gain $\beta$, and due to the lack of a complementary (PNP+NPN) process. Without this, pull-up resistors of finite value must be used for bias currents, and their finite resistance leads to finite gain. Use (Fig. 5) of very large pull-up resistances results in difficulties in controlling DC bias, difficulties which are addressed though use of an off-wafer common-mode bias feedback control loop.

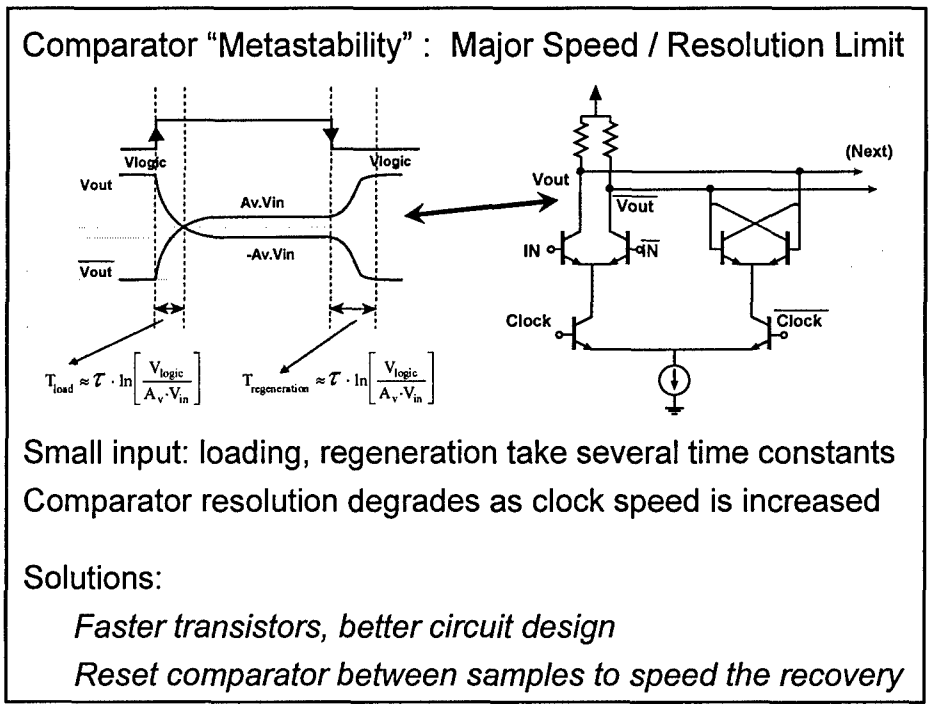



Figure 6: Metastability and dynamic hysteresis errors.

The aforementioned limitations in noise suppression, while significant, are thus addressed and resolved by appropriate circuit design. A more fundamental problem relates to the dynamic resolution of the latched comparator (fig. 6). Two significant limitations are dynamic hysteresis and metastability. Dynamic hysteresis (fig. 6) arises because finite time required to reset the latch between clocking events. This reset transient may overwhelm a small input signal, causing the latch to hold the prior state. Metastability (fig. 6 and fig. 7) results from the modulation of latch output risetime by the strength of the input signal.

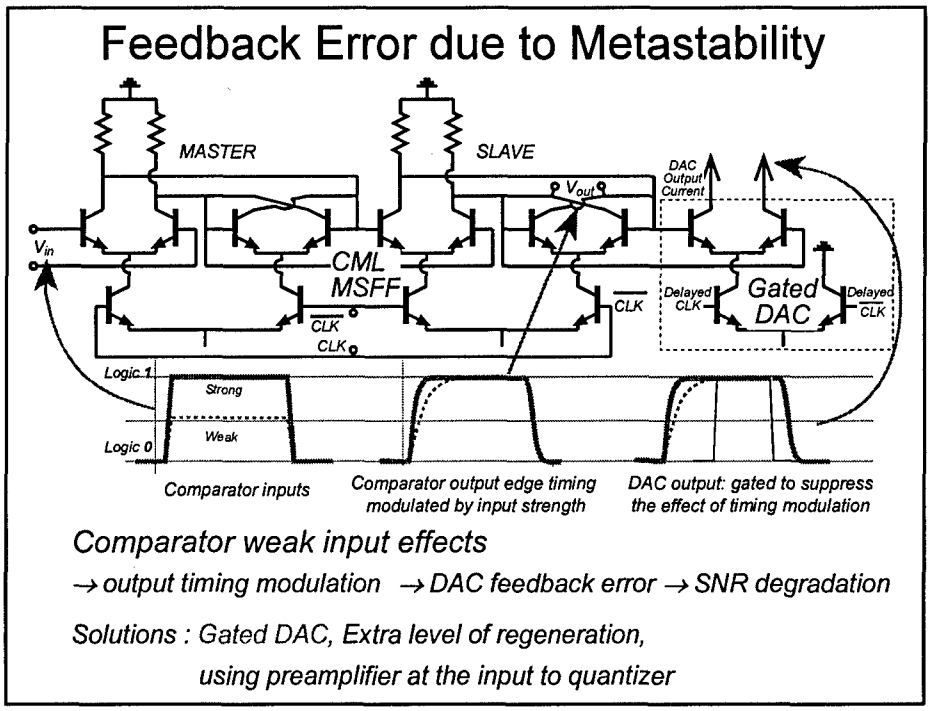



Figure 7: Metastability errors and their partial suppression by latch gating.

This modulation of signal risetime modulated the amount of charge fed back by the DAC to the $\Delta-\Sigma$ input. As an feedback error, the magnitude of this error is not suppressed by the loop gain. Metastability thus is a serious limit to $\Delta-\Sigma$ resolution. In the first generation $\Delta-\Sigma$ designs, the magnitude of metastability errors was partially suppressed (fig. 8) through gating of the DAC feedback signal, eliminating much of the signal during the time when the risetime modulation is most significant.

Linearity and thermal noise of the input stage are additional limits to both the ADC spurious-free dynamic range and the signal/noise ratio. The first generation designs used Caprio's cell to reduce input stage intermodulation. Bias currents and resistor values in the input stage were selected to keep the input thermal noise below the quantization noise.

Figure 8 shows a simplified circuit schematic, while figure 9 shows a die photograph. The IC has approximately 200 transistors, and is fabricated in the transferred-substrate technology. The dimensions and epitaxial layers are such that typical transistors have 200 GHz $f_\tau$ and $f_{\max}$, while the latched comparators have a maximum 75 GHz clock frequency.

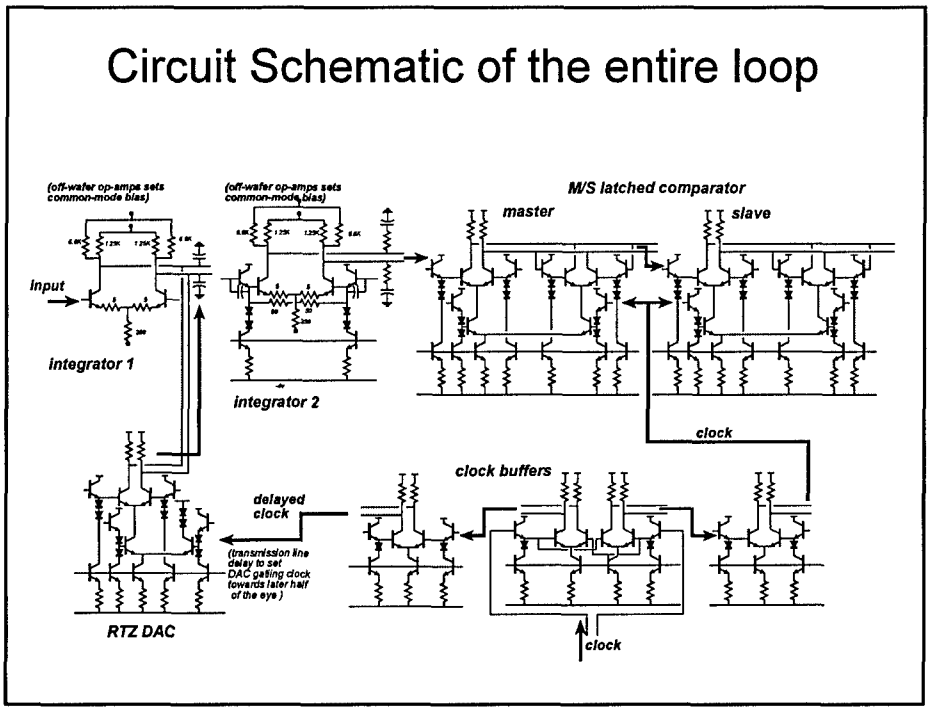



Figure 8: Simplified IC schematic

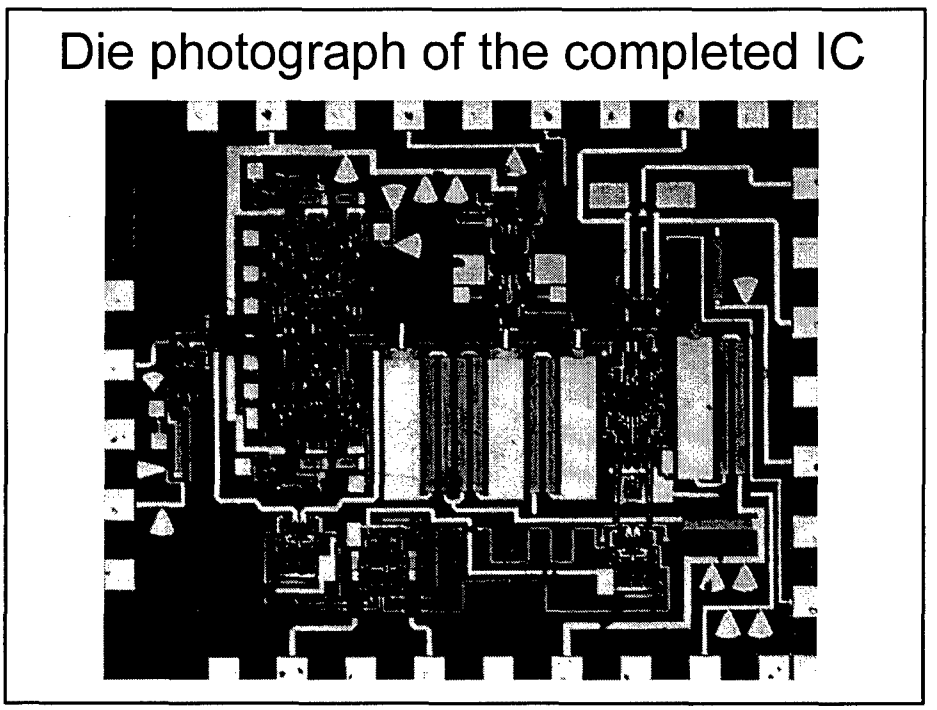



Figure 9: Die photograph, first generation design

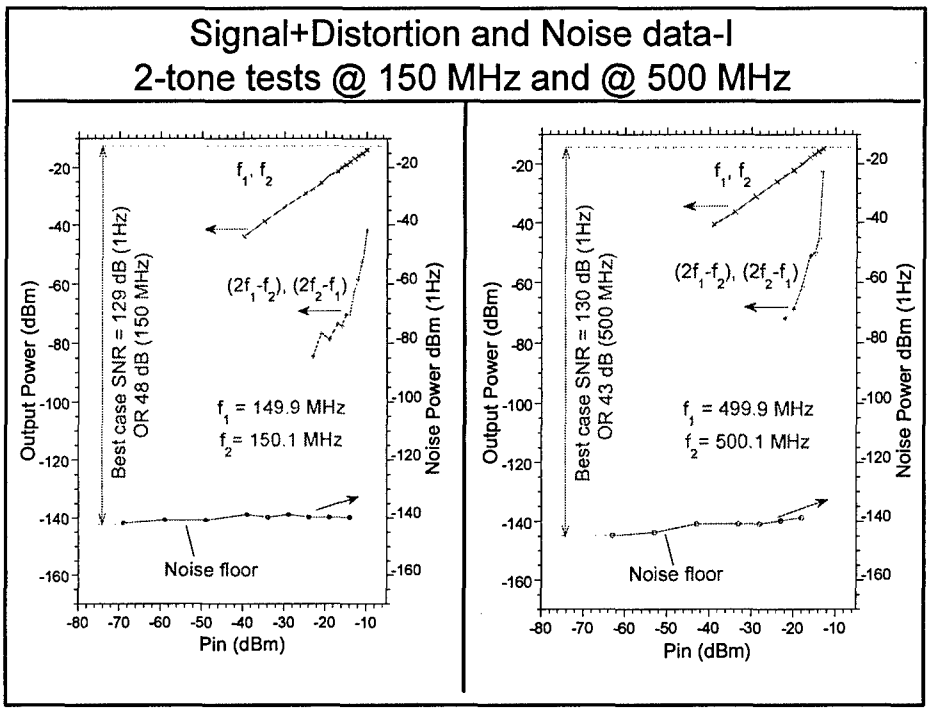



Figure 10: Performance, first-generation design.

Figure 10 shows the measured performance with 2 tone testing. Because the 20 GHz data stream could not be captured digitally, the output was instead measured by analog filtering and measurement on a spectrum analyzer. There is consequently significant error in the measurements. Beyond this point, the system resolution was well below that expected from simulations.

**Third-Generation Delta-Sigma ADC**

Subsequent to the design above, 2 additional design cycles of the $\Delta - \Sigma$ ADC were pursued. The 2nd generation design and the third-generation design used similar circuit design improvements; the 2 designs differ primarily in that the 2nd generation design was based upon transferred-substrate HBT technology, while the 3rd generation design used a more conventional mesa HBT process. This 3rd-generation design was motivated by continuing difficulties in obtaining acceptable process yield in large ICs in the transferred-substrate process. Indeed, the overall program progress was delayed by numerous failures in IC processing. No 2nd-generation ICs were completed, hence the report will focus on the 3rd generation design.

In order to obtain acceptable yield on the 3rd generation designs, a mesa HBT process was employed. The objectives were to obtain high yield on devices, good RF performance (200 GHz ft and fmax), and low Ccb. These devices use dimensions that had

earlier shown the best yield in the transferred-substrate technology (0.7 um emitters). To obtain acceptably low Ccb, a narrow base mesa (1.7 - 2.1 um width ) is employed, and low resistance Pd/Ti/Pd/Au base-ohmic contacts were used for reduced Rbb. Figure 11 summarizes the mesa HBT technology performance circa Spring 2002. At that time transistors with 200 GHz $f_\tau$ and $f_{\max}$ , high breakdown, and high current density, could be fabricated.

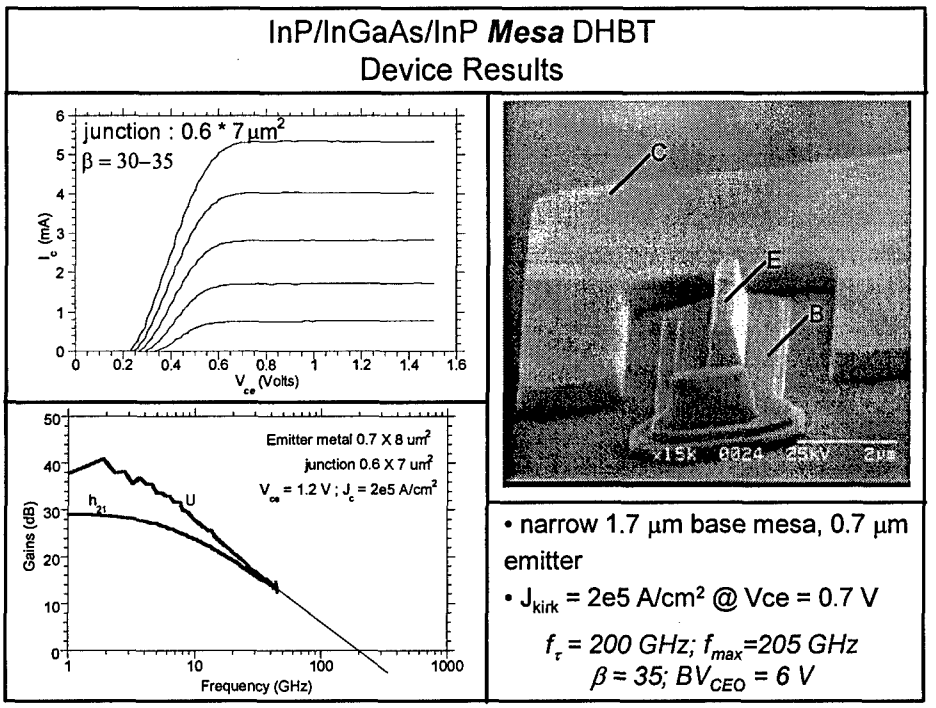



Figure 11: Performance of narrow-mesa DHBT technology circa May 2002

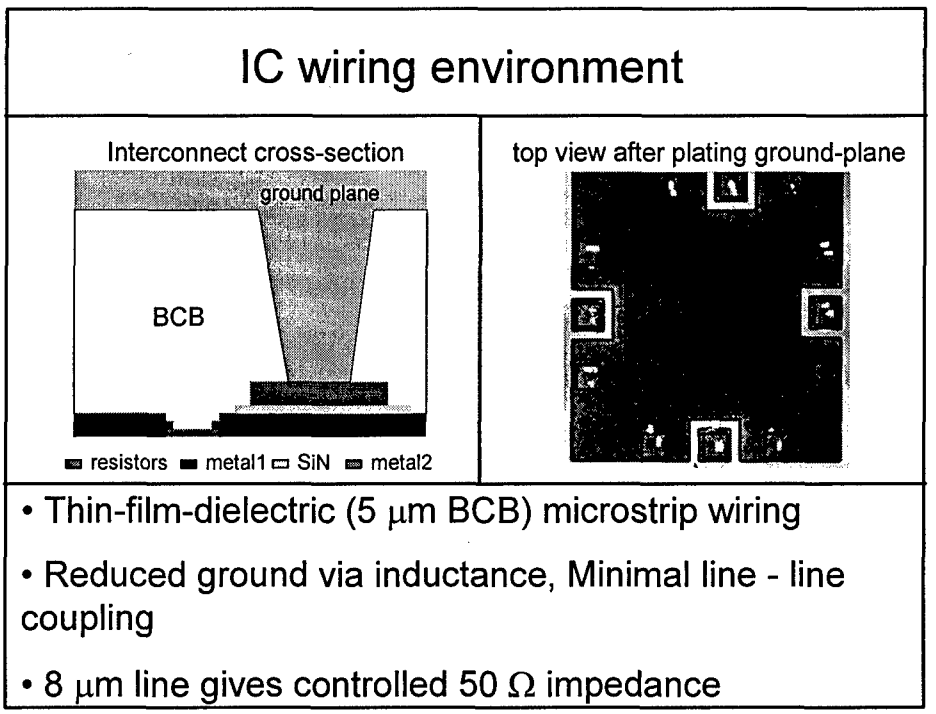
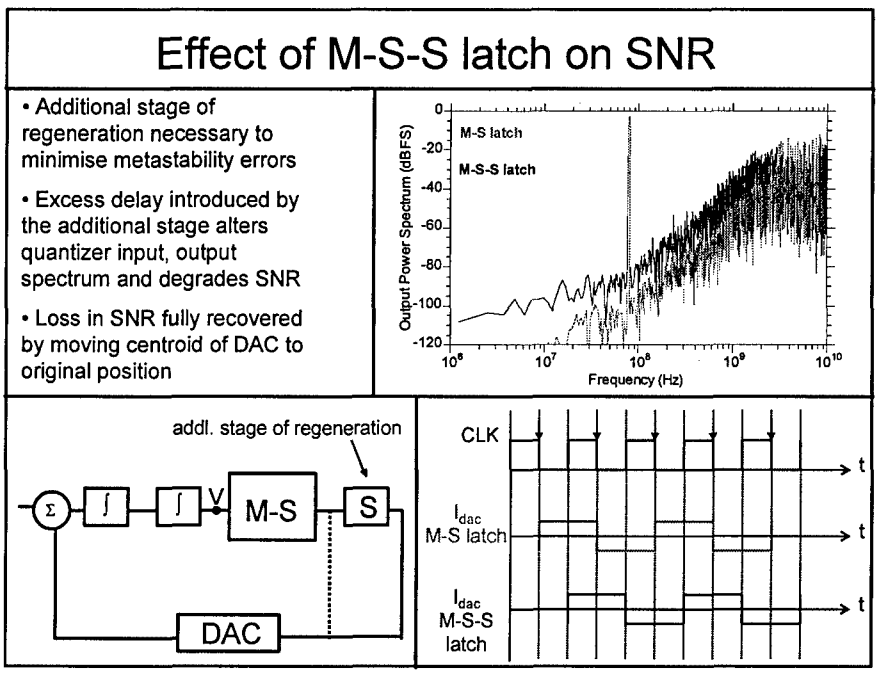



Figure 12: Thin-film microstrip wiring environment and ground plane in Narrow-mesa technology

The IC technology also employed a thin-film microstrip wiring environment (figure 12). This feature was carried over from the transferred-substrate process. Normal mixed signal ICs use random wiring, which is simple to fabricated. This however gives uncontrolled line impedances and varying degrees of circuit coupling through ground bounce. The thin film environment provides and controlled and predictable Zo for all interconnects, and eliminates circuit-circuit coupling through nonzero ground system impedance.



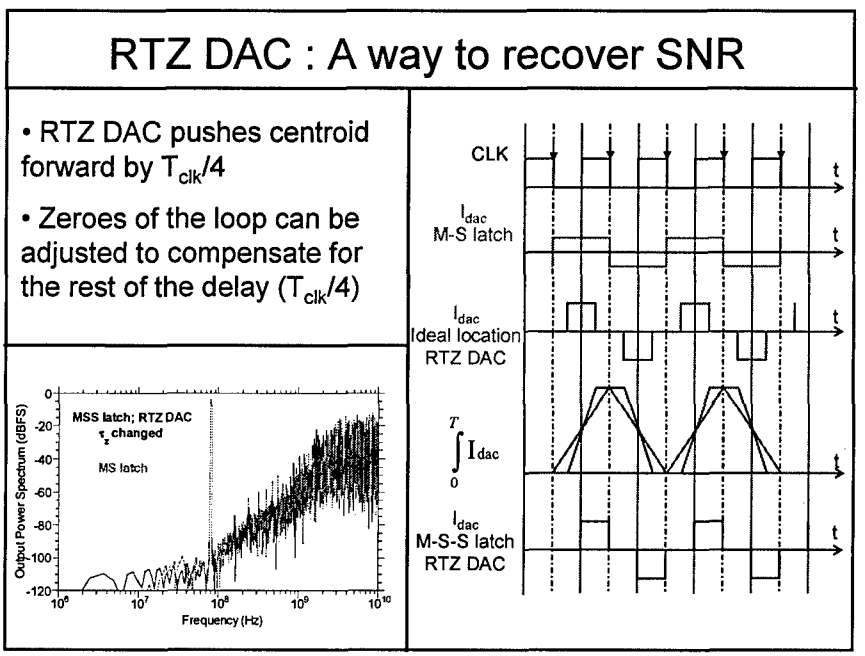




Figure 13: An MSS latch reduces metastability errors but degrades SNR through increased loop delay. This excess delay can be compensated for by addition of a gated (RTZ) latch and additional zeros inserted into the loop transfer function.

One key change between the 1st and 3rd generation design (fig. 13) was the method of reducing metastability errors. In the 3rd generation design, this is provided through addition of a 2nd stage of regeneration in the form of an MSS latch. The excess delay thus introduced can degrade the SNR; this excess delay is reduced through use of an RTZ DAC and partially compensated for by insertion of a zero in the loop transfer function.

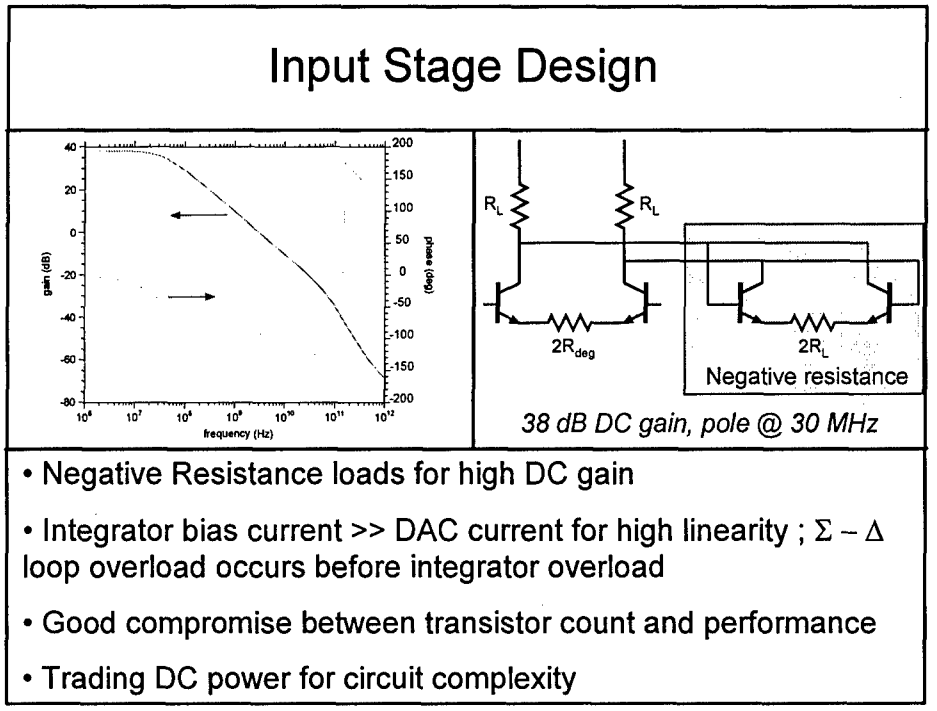



Figure 14: Negative-resistance loading for high integrator gain at low frequencies.

A second significant design change was in the integrators. In the 3rd-generation design (Fig. 14) high gain at low frequencies is obtained by using negative-resistance loading of the Gm cells. This proved significantly less sensitive to power supply voltage than the common-mode feedback technique.

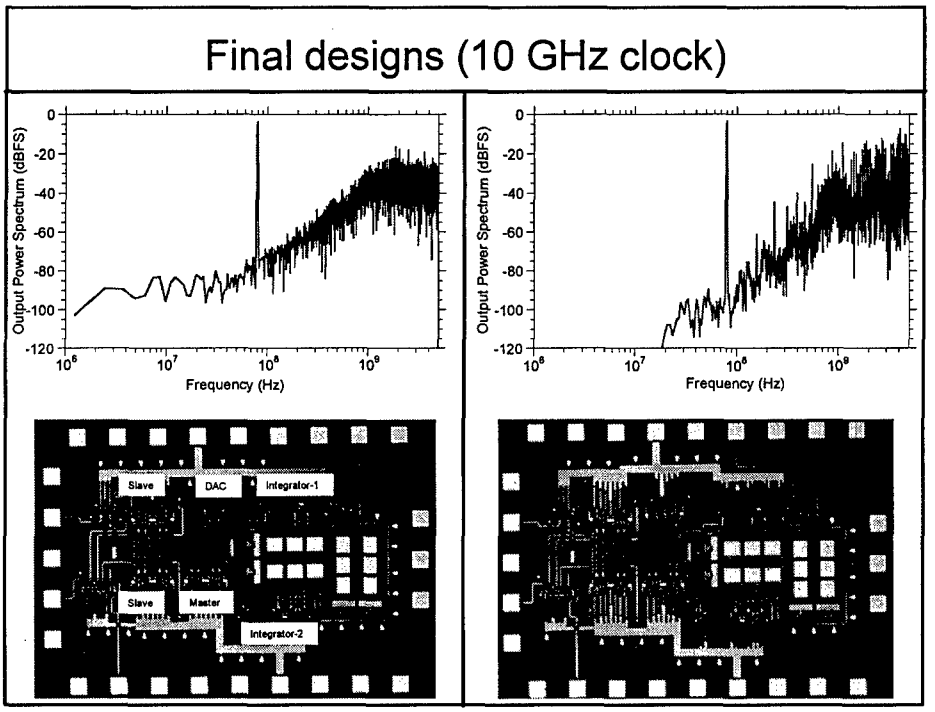


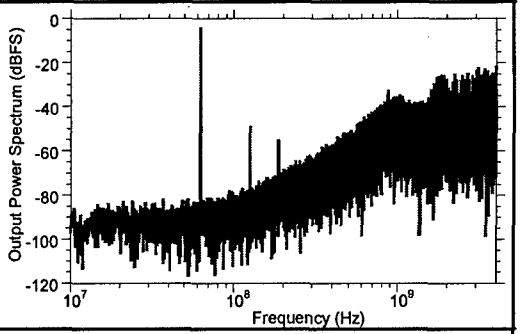

Figure 15: Completed 3rd-generation $\Delta - \Sigma$ ADCs with NRZ and RTZ DACs.

Figure 15 shows the completed 3rd-generation DACs (photographs taken before deposition of the ground planes) , showing designs both with and without the RTZ DAC. The ICs contain approximately 75 transistors.

## SNR and # of bits of resolution

For an equivalent Nyquist-rate ADC, SNR and effective # of bits of resolution, ENOB, are related by

ENOB = (SNR-1.76)/6.02




| | | Noise power measured at upper band edge | | | | Noise power integrated to signal frequency | | | |
|---|---|---|---|---|---|---|---|---|---|
| Signal Frequency, Hz | Equivalent Sampling rate, S/s | SNR, dB 61 kHz | SNR, dB 1 Hz | SNR, dB Nyquist | ENOB | SNR, dB 61 kHz | SNR, dB 1 Hz | SNR, dB Nyquist | ENOB |
| 6.25e7 | 1.25e8 | 85.37 | 133.23 | 55.3 | 8.89 | 87.54 | 135.39 | 57.4 | 9.25 |
| 1.25e8 | 2.5e8 | 81.3 | 129.16 | 48.2 | 7.71 | 84.8 | 132.65 | 51.7 | 8.29 |
| 2.5e8 | 5e8 | 70.7 | 118.56 | 34.6 | 5.45 | 76.3 | 124.15 | 40.2 | 6.38 |

Figure 16: Tabulation of measured performance

Because the clock rate was reduced to 8 GHz in the 3rd generation design, the digital output could be captured using commercially available high speed digital electronics developed for the 10 Gb/s optical fiber transmission market. The data is then captured on a logic analyzer, downloaded to a PC, and the FFT computed. Measurement results are summarized in figure 16. At a signal frequency of 125 MHz (equivalent to a Nyquist converter operating at 250 Megasamples per second), an effective resolution of 8.3 bits was obtained.

**Staff supported**

S. Jaganathan (Ph.D. 2000)

Sundararajan Krishnan (Ph.D. 2002)

Thomas Mathew (Ph.D. 2001)

C. Serhan (M.S. 2000)

## Publications associated with contract

| | | | | |
|---|---|---|---|---|
| 1 | 1999 | M.J.W. Rodwell, Q. Lee, D. Mensa, J. Guthrie, Y. Betser, S.C. Martin, R.P. Smith, S. Jaganathan, T. Mathew, P. Krishnan, C. Serhan, and S. Long, "Transferred-Substrate Heterojunction Bipolar Transistor Integrated Circuit Technology." | Eleventh International Conference on Indium Phosphide and Related Materials, Davos, Switzerland, pp. 1-6, May 16-20. | **Conference Paper (Invited)** |
| 2. | 2000 | S. Jaganathan, D. Mensa, T. Mathew, Y. Betser, S. Krishnan. Y. Wei. D. Scott, M. Urteaga, M. Rodwell, "A 18 GHz Continuous Time $\sum$ - $\Delta$ Modulator Implemented in InP Transferred Substrate HBT Technology." | *22nd Annual IEEE GaAS IC Symposium 2000*, Seattle, WA, November 5-8. | **Conference Paper** |
| 3. | 2001 | M. Urteaga, D. Scott, M. Dahlstrom, Y. Betser, S. Lee, S. Krishnan, T. Mathew. S. Jaganathan. Y. Wei, M.J.W. Rodwell, "Ultra High Speed Heterojunction Bipolar Transistor Technology." | *2001 GOMAC Conference*, San Antonio, Texas, March 5-8. | **Conference Paper (Invited)** |
| 4. | 2001 | M. Urteaga, D. Scott, M. Dahlstrom, Y. Betser, S. Lee, S. Krishnan, T. Mathew. S. Jaganathan. Y. Wei, M.J.W. Rodwell, "Ultra High Speed Heterojunction Bipolar Transistor Technology." | *2001 GOMAC Conference*, San Antonio, Texas, March 5-8. | **Conference Paper (Invited)** |
| 5. | 2001 | M.J.W. Rodwell, M. Urteaga, Y. Betser, D. Scott, M. Dahlstrom, S. Lee, S. Krishnan, T. Mathew. S. Jaganathan. Y. Wei, D. Mensa, J. Guthrie, R. Pullela, Q. Lee, B. Agarwal, U. Bhattacharya, S. Long "Scaling of InGaAs/InAlAs HBTs for High Speed Mixed-Signal and mm-Wave ICs" | *International Journal of High Speed Electronics and Systems*, Vol. 11, No. 1, pp. 159-215. | **Journal Paper** |
| 6. | 2001 | S. Jaganathan, S. Krishnan, D. Mensa, T. Mathew, Y.Betser, Y. Wei, D. Scott, M. Urteaga, M. Rodwell. "An 18 GHz continuous time sigma-delta analog-digital converter implemented in InP transferred substrate HBT technology" | *IEEE Journal of Solid State Circuits,* Vol. 36, No. 9, pp. 1343-1350, September. | **Journal Paper** |
| 7. | 2001 | M. Rodwell, S. Long, M. Urteaga, T. Mathew, D. Scott, S. Lee, Y. M. Kim, Y. Wei, N. Parthasarathy, M. Dahlstrom, H.J. Kim, Z. Griffith, "High Speed InP-Based Heterojunction Bipolar Transistors." | *28th International Symposium on Compound Semiconductors 2001 (ISCS2001)*, Komaba Campus, University of Tokyo, October 1-4. | **Conference Paper (Invited)** |

| | | | | |
|---|---|---|---|---|
| 8. | 2001 | M.J.W. Rodwell, Miguel Urteaga, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S.C. Martin, R.P. Smith, S. Jaganathan, T. Mathew, P. Krishnan, S. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, Denis Scott, Mattias Dahlstrom, "Submicron Scaling of HBTs." | *IEEE Transactions on Electron Devices,* Vol. 48, No. 11, p. 2606-2624, November. | **Journal Paper (Invited)** |
| 9. | 2003 | Sundararajan Krishnan, Dennis Scott, Miguel Urteaga, Zachary Griffith, Yun Wei, Mattias Dahlstrom, Navin Parthasarathy, Mark Rodwell, "An 8-GHz Continuous-Time Sigma-Delta Analog-Digital Converter in an InP-based DHBT Technology." | *To be published International Microwave Symposium,* Philidelphia, June 8-10. | **Conference Paper** |
| 10 | 2003 | Sundararajan Krishnan, Dennis Scott, Miguel Urteaga, Zachary Griffith, Yun Wei, Mattias Dahlstrom, Navin Parthasarathy, Mark Rodwell, "An 8-GHz Continuous-Time Sigma-Delta Analog-Digital Converter in an InP-based DHBT Technology." | *Submitted to IEEE-MTT transactions* . | **Journal Paper** |

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